Les memristors :
un nouveau paradigme en nanoélectronique

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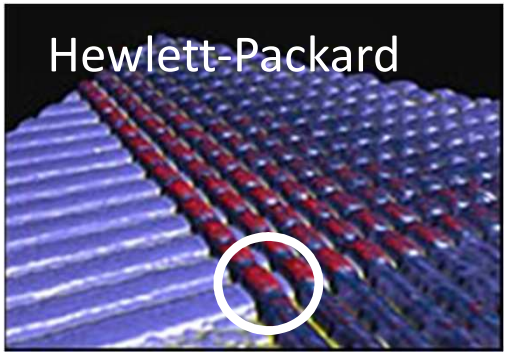
INVESTISSEMENTS D'AVENIR

Le memristor : définition

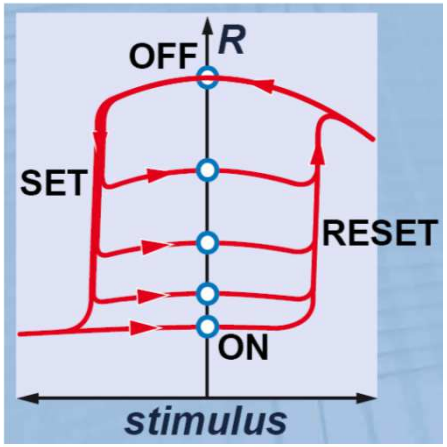
» **Un memristor est une résistance « à effet mémoire »**

- nanométrique
- analogique (entre R_{ON} et R_{OFF})
- non-linéaire
- non-volatile (mémoire)

2008



< 30x30 nm²



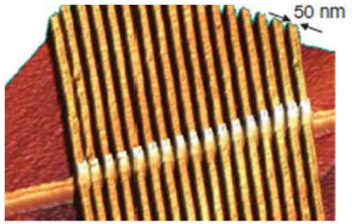
L. O. Chua, "memristor – the missing circuit element" IEEE Trans. Circuit Theory (1971)

Strukov, Snider, Stewart & Williams, Nature 453 (2008)

Memristor : applications

» **Mémoires binaires ou multi-états**

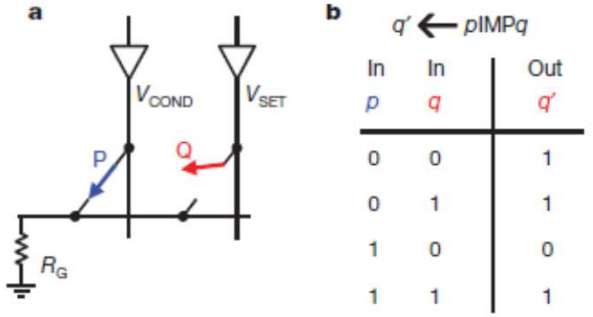
– Memristor = composant non-volatile



» **Fonctions logiques & Architectures reconfigurables**

– Memristor = commutateur ON/OFF

+ mémoire non-volatile



» **Réseaux de neurones artificiels**

– Memristor = composant analogique non-volatile

= nano-synapse

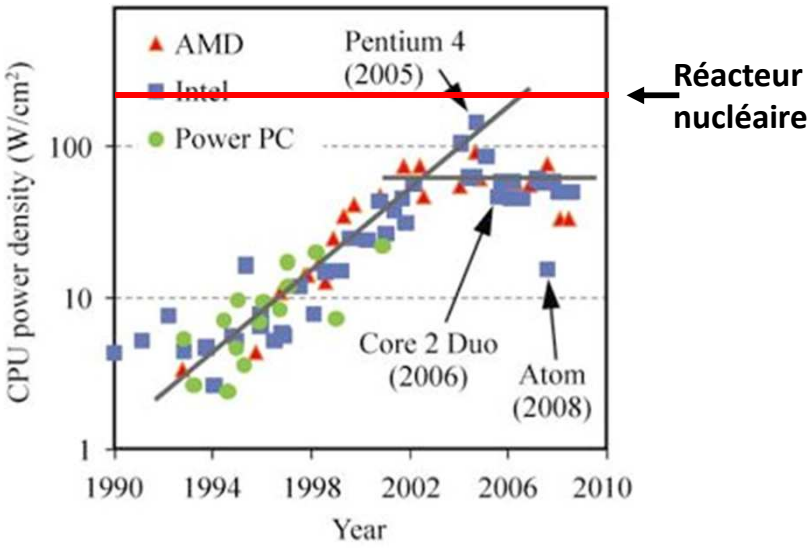
Premier exemple : utilisation de memristors en tant que mémoires binaires

Processeur non-volatile

CNRS-PEPS NVCPU : IEF / UMφ CNRS-Thales / LIRMM

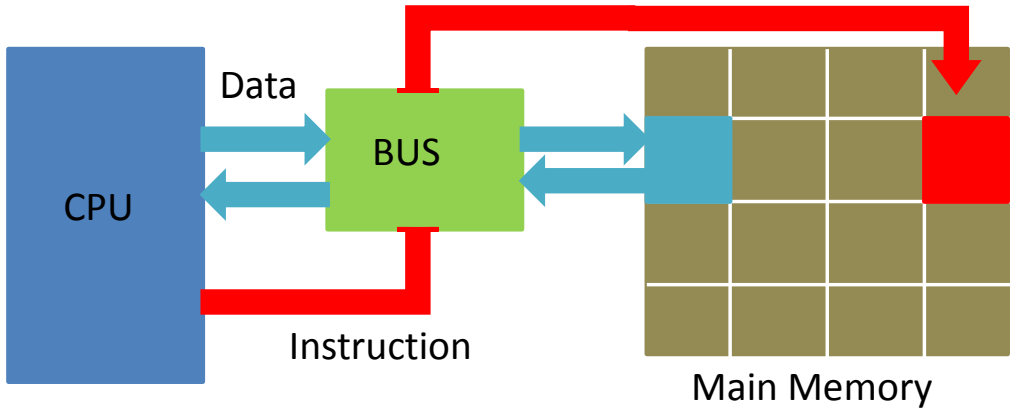
Vers des unités de calcul ultra-rapides et ultra-faible consommation

Power Crisis of CPU



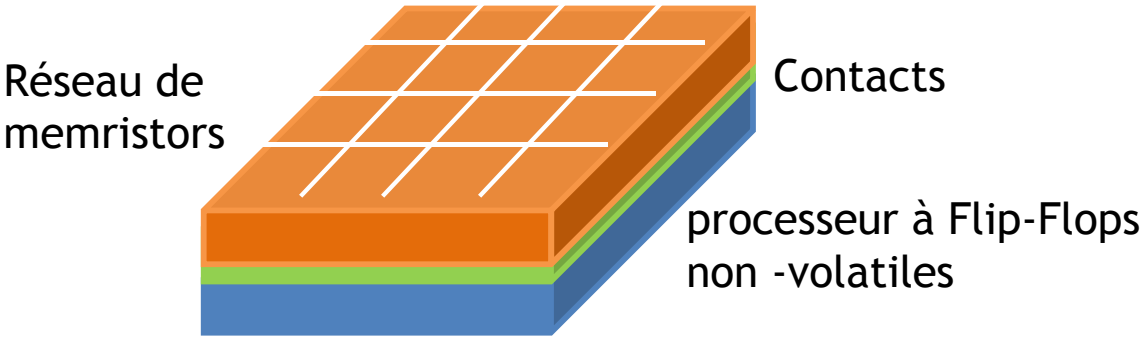
Source: Intel (2007)

Architecture de calcul conventionnelle



En techno 22 nm, changer 1 bit dans un transistor a pour coût énergétique:
~ 1 femtojoule (10^{-15} J)
Transférer une donnée de 1-bit sur le silicium coute:
~1 picojoule/mm (10^{-12} j/mm)

Mémoire RAM à réseau de composants non-volatiles (Memristors)



Ultra faible conso ('0' standby+ presque '0' en transfert)
Ultra haute performance (>10Gb memoire + >10GHz)

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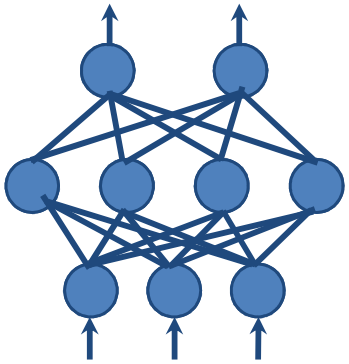
Deuxième exemple : memristor en tant que nano-synapse

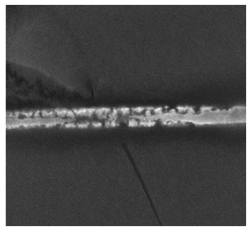
réseaux de neurones artificiels sur puce



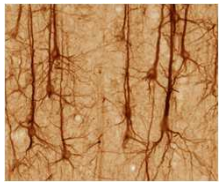
Architecture massivement parallèle et uniforme

- rapidité
- faible consommation
- tolérance aux défauts

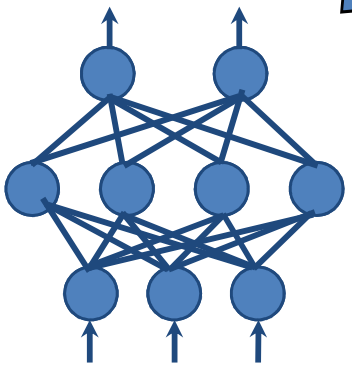
Convergence : vers les réseaux de neurones artificiels sur puce

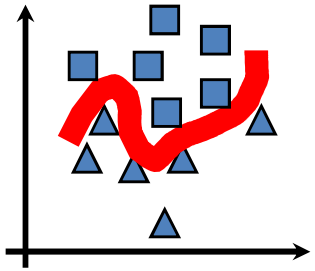


Contraintes technologiques



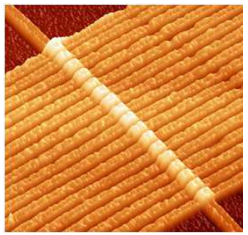
Neurobiologie





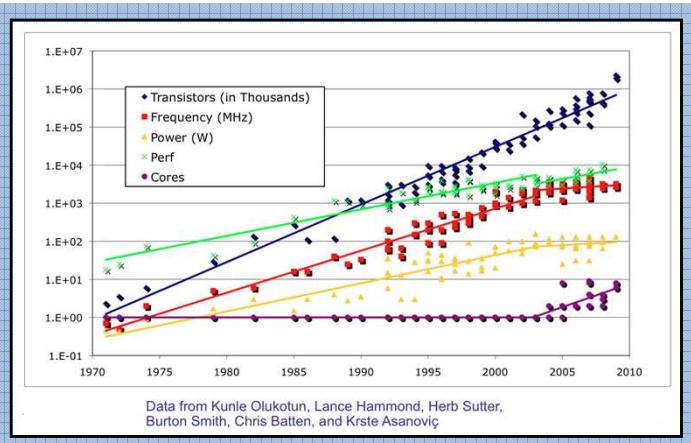
Machine Learning

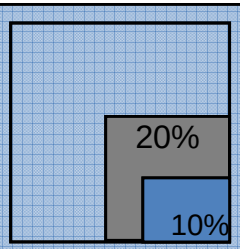
Applications



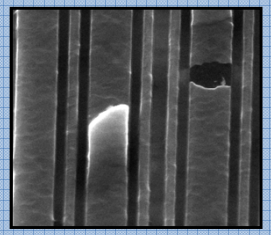
Nanotechnologies

Contraintes technologiques : puissance consommée et défauts

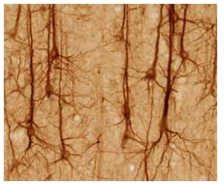




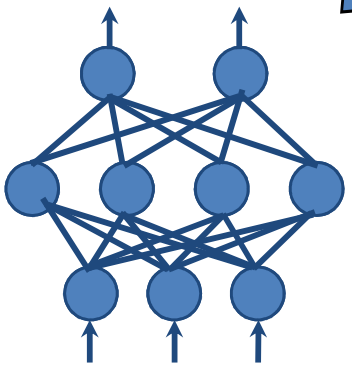
Dark Silicon

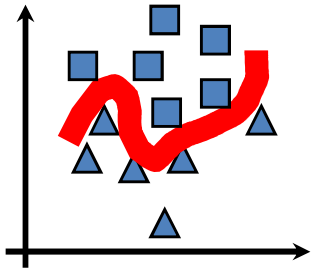


Défauts



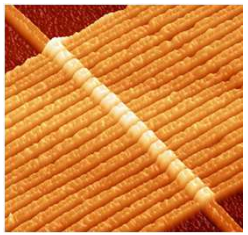
Neurobiologie





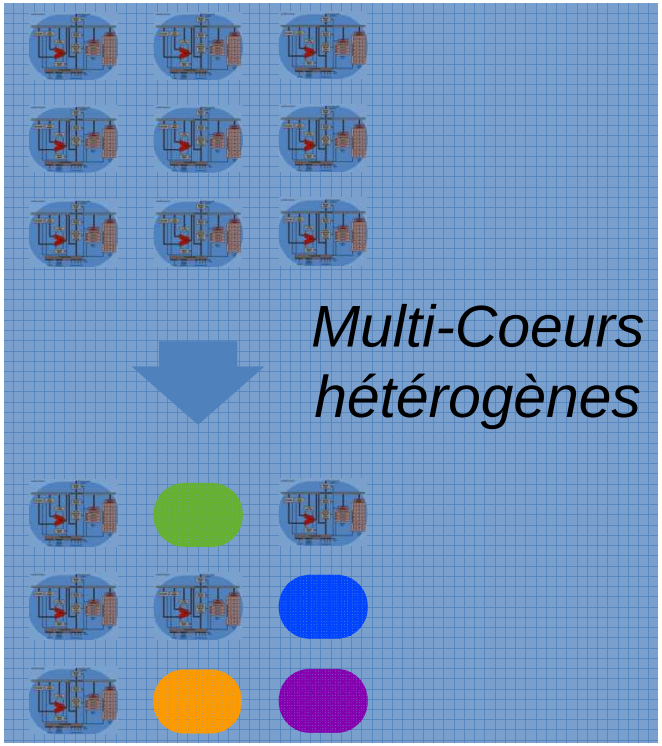
Machine Learning

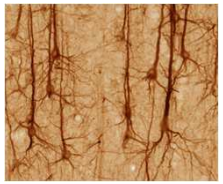
Applications



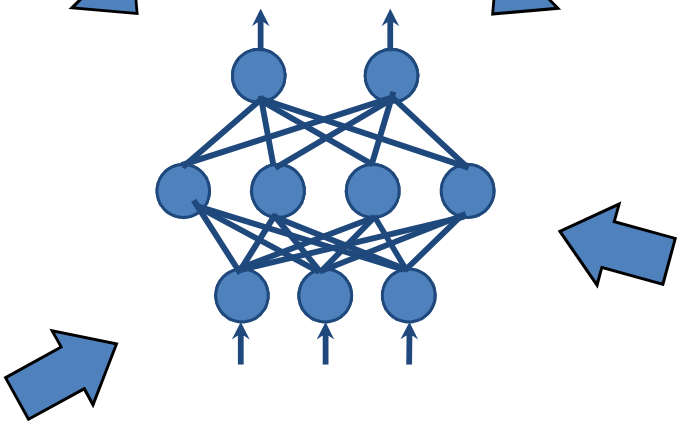
Nanotechnologies

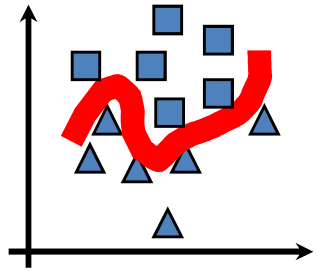
Accélérateurs tolérants aux défauts





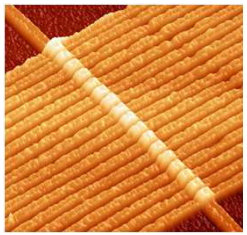
Neurobiologie





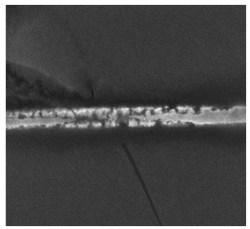
Machine
Learning

Applications

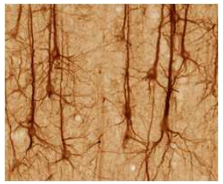


Nanotechnologies

Applications du futur : recognition, mining & synthesis

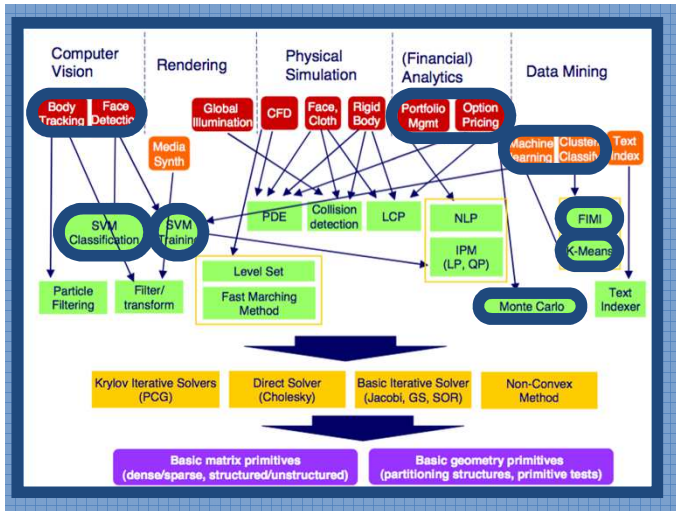


Contraintes technologiques

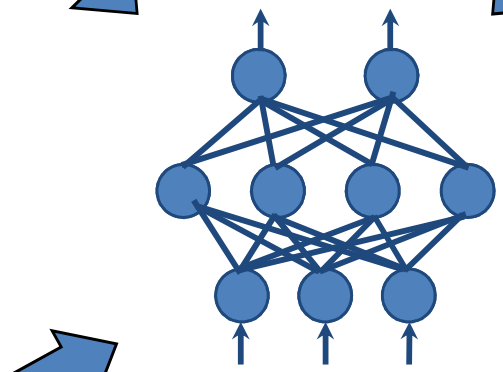


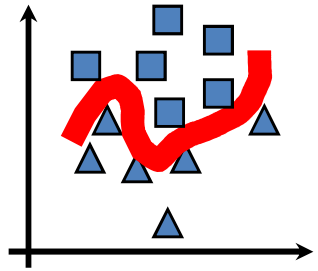
Neurobiologie

RMS

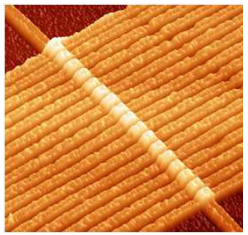


Applications



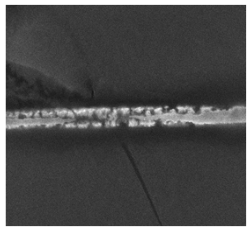


Machine Learning



Nanotechnologies

Progrès en neurobiologie : réalisation de taches complexes avec des réseaux de neurones



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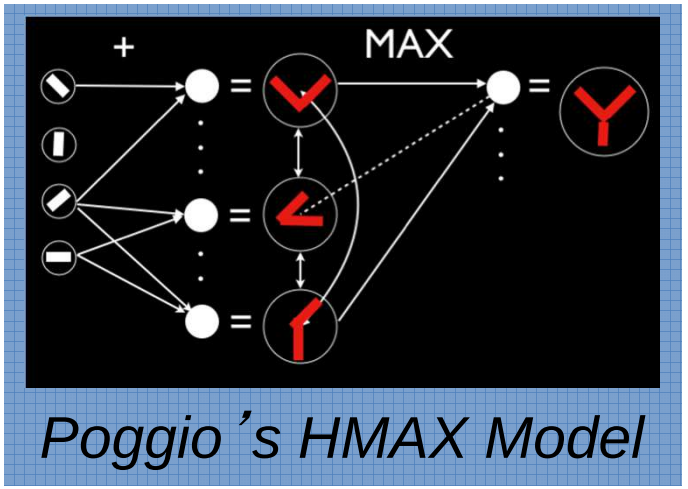
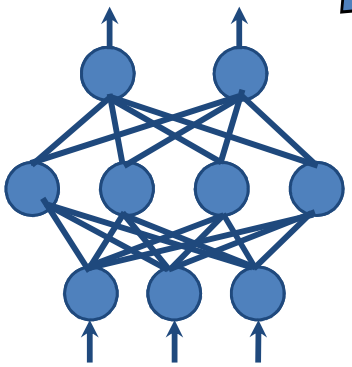
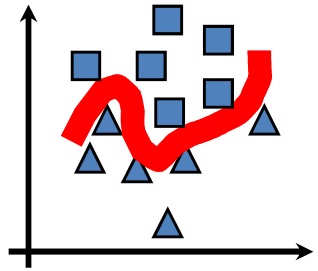
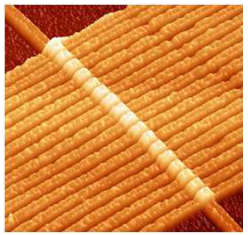






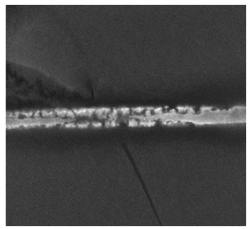
Machine Learning

Applications



Nanotechnologies

Réseaux large échelle



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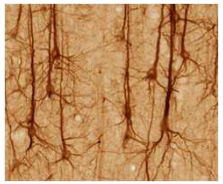
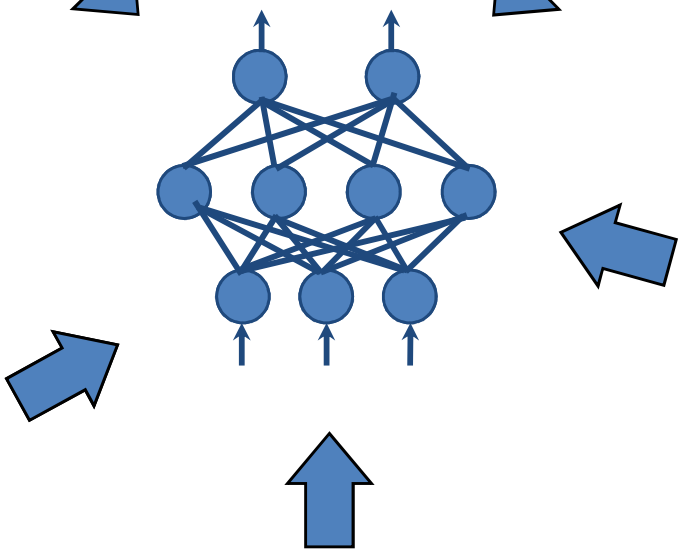
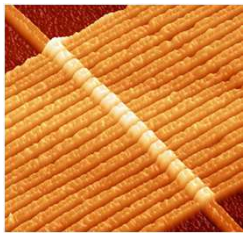


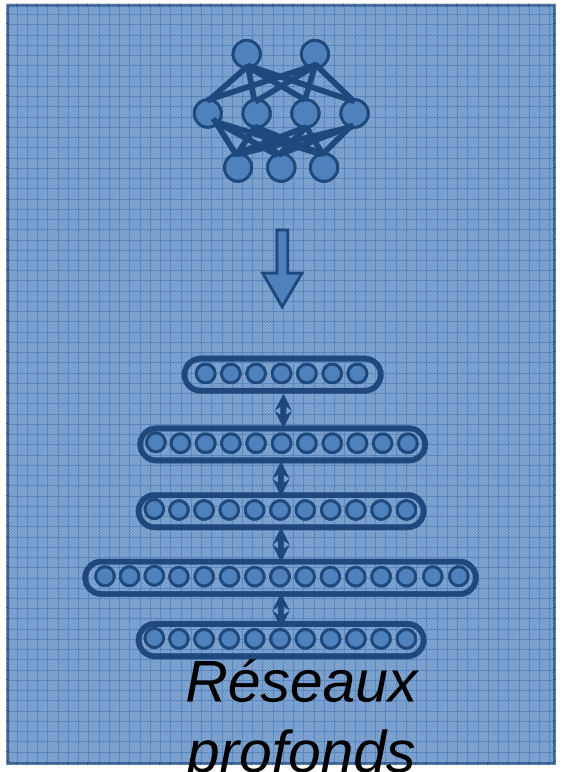
Neurobiologie



Applications

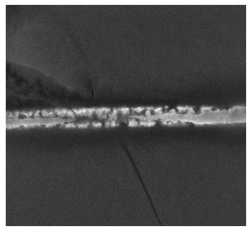


Nanotechnologies



Machine Learning

un memristor = une nano-synapse : vers des réseaux ultra-denses



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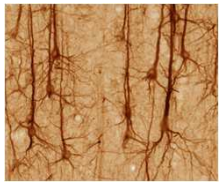
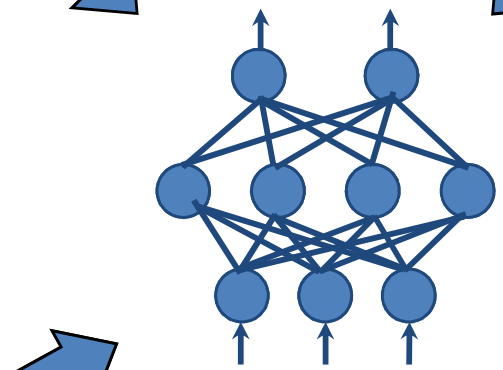
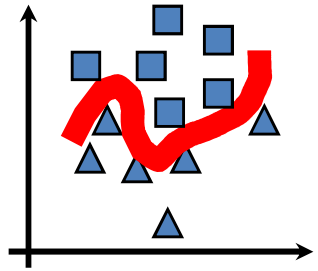


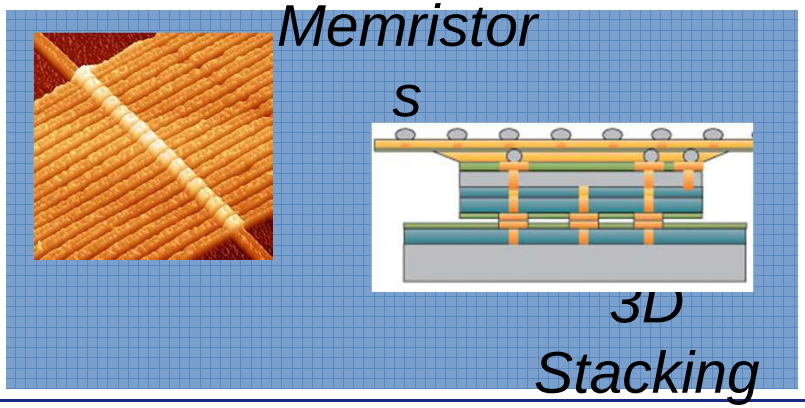
Neurobiologie





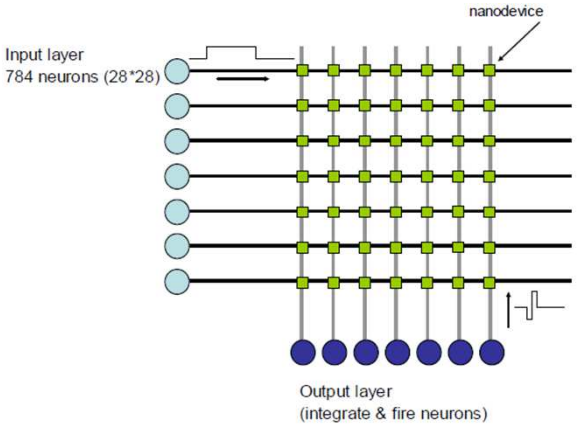
Machine Learning

Applications

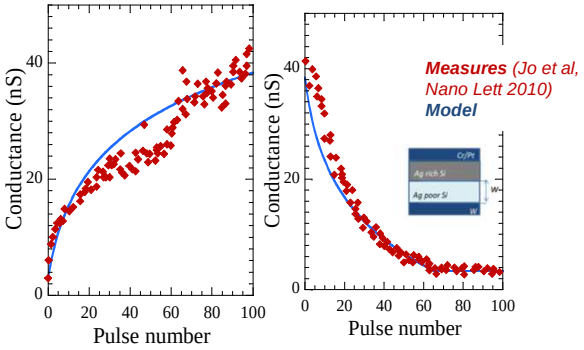


Démonstration du potentiel des architectures neuro-inspirées utilisant les memristors (CEA List / IEF-Orsay)

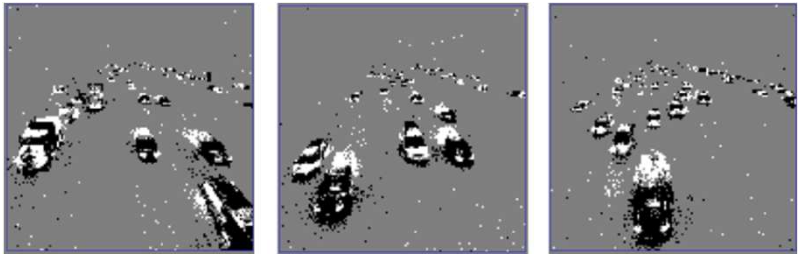
conception et simulation de systèmes neuro-inspirés ultra-adaptatifs



Architecture

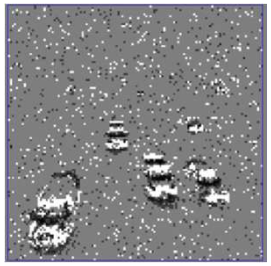


Modèle des composants



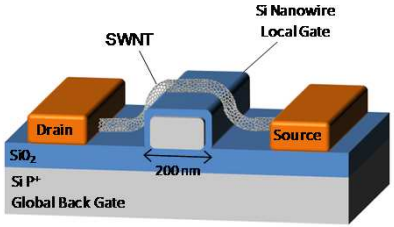
On présente 10 min. vidéo d'une autoroute.
Le système devient compteur de véhicules, avec perf. de 98%

- Apprentissage non supervisé pour s'adapter à divers problèmes
- Développement d'un simulateur spécialisé pour le nanodesign (*Xnet)*
- Applications image, vidéo, son

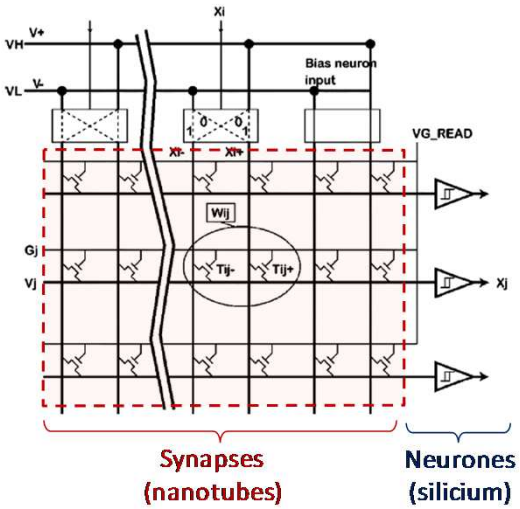


Extrême robustesse du système (bruit, variabilité)

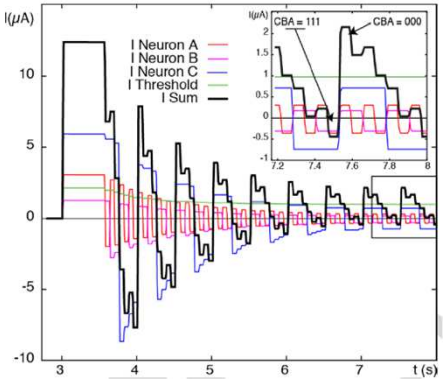
Réalisation de prototypes simples (IEF / CEA-Lem / CEA-List)



physique des composants

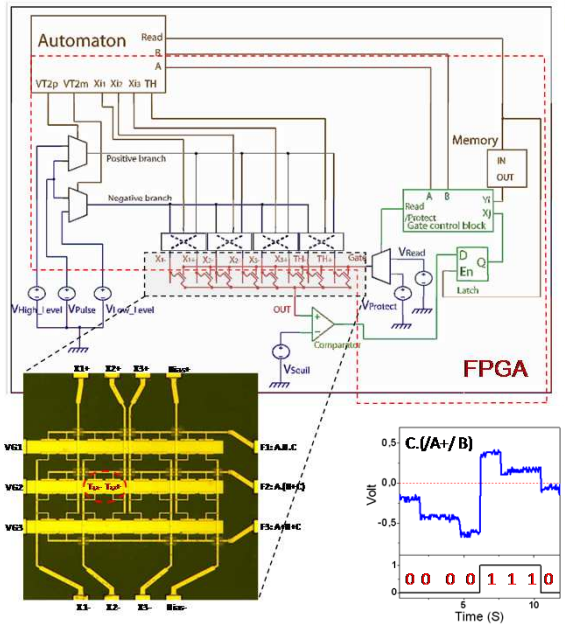


topologie du circuit & règles d'apprentissage



Modélisation et simulation

Exemple d'interactions sur les circuits à apprentissage



ANR PANINI Project

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Prototypes simples de circuits hybrides

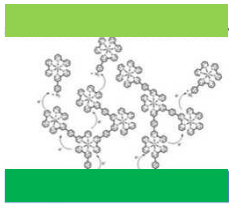
NanoSaclay
Laboratoire d'Excellence en Nanosciences et Nanotechnologies

Objectifs dans le cadre du labex Nano-Saclay :

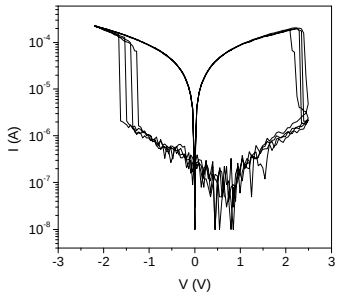
Vers des circuits ultra-performants et ultra-faible consommation
co-intégrés CMOS/memristors

Nouveaux types de memristor

UMφ CNRS-Thales, CEA-LEM,…



- Memristor organique (NOM-FET, CNT-FET)
- Memristor spintronique

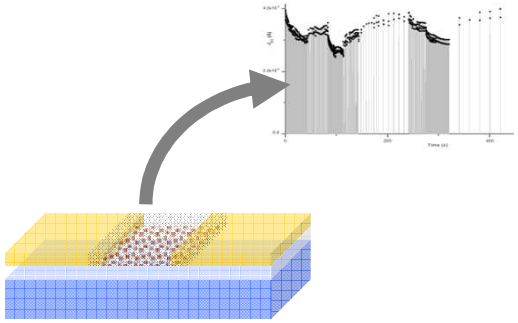


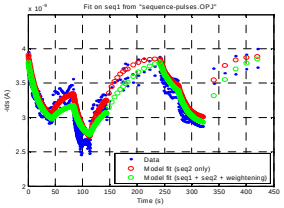
- Memristor ferroélectrique
- …

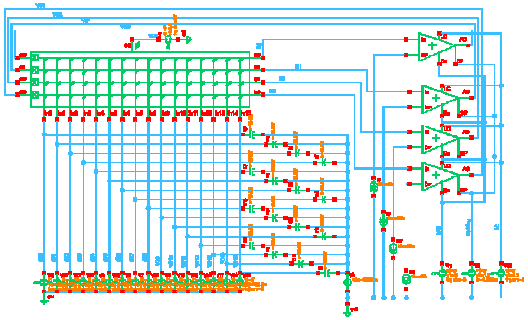
Rapidité, faible consommation, fiabilité, compréhension des mécanismes physiques

Plateforme de modélisation

CEA-LIST / IEF-Orsay /CEA-LEM / IEMN / ….

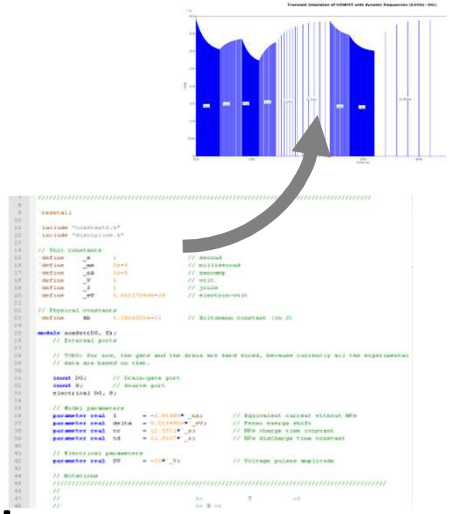






Plateforme CAO

Outils standards



- **Permettre l'évaluation d'une variété de nano-technologies candidates**
- **Modélisation hybride avec le CMOS pour exploration d'architectures**
  - Intégration avec les outils de conception standards

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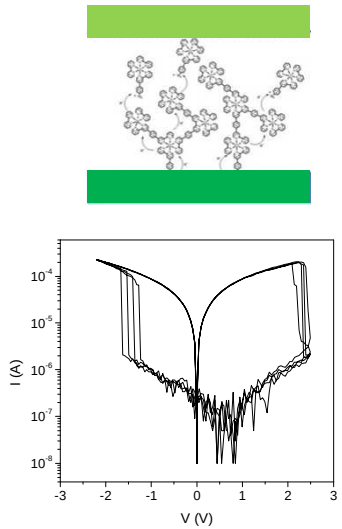
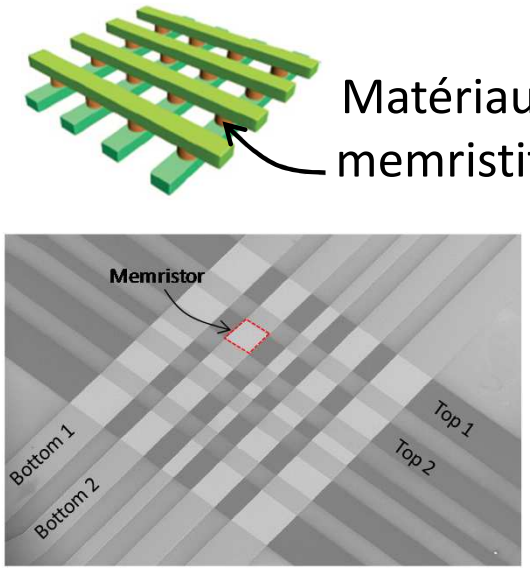
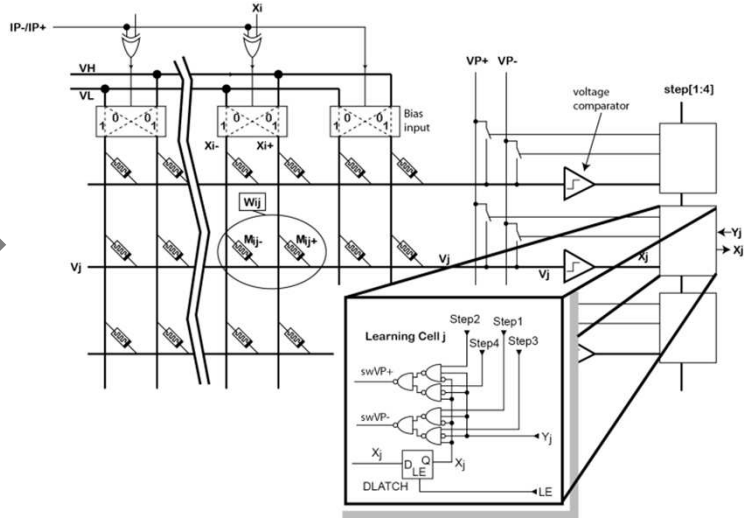
Méthode



chimie & physique des composants



Integration en réseau

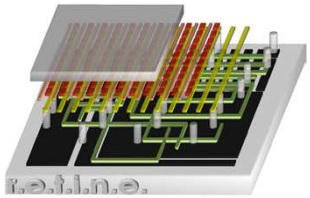


topologie du circuit & règles d'apprentissage

Liens étroits nécessaires entre physiciens et concepteurs de circuits

Modélisation & simulation

Prototypes de circuits hybrides



Cointégration nano/CMOS

Une équipe interdisciplinaire

Nanodevices

Unité Mixte de Physique CNRS Thales

CEA-IRAMIS@NanoINNOV

…

Nanodesign

Institut d'Electronique Fondamentale

Laboratoire d'Intégration des Systèmes et desTechnologies

INRIA Saclay Research Center

Thales Research & Technology

…